AMENDMENTS TO THE CLAIMS

1. (Original) A polysilicon etching method comprising steps of:

preparing a semiconductor substrate having an insulating film with a protrusion formed on one principal surface of said substrate and a polysilicon layer deposited on said insulating film and covering the protrusion;

forming a resist layer on the said polysilicon layer, said resist layer having a predetermined pattern not covering at least a portion of side walls of the protrusion;

performing a first plasma etching process of etching said polysilicon layer by using mixture gas of HBr and Cl_2 and said resist layer as a mask to leave said polysilicon layer having a pattern corresponding to said resist layer and polysilicon residues made of a portion of said polysilicon layer on the side walls of the protrusion; and

performing a second plasma etching process of removing the polysilicon residues by using single gas of HBr and said resist layer as a mask.

2. (Original) A polysilicon etching method according to claim 1, wherein said second plasma etching process is performed at a pressure in a range of 5.0 to 10.0 mTorr.

3. (Original) A polysilicon etching method according to claim 1, wherein said second plasma etching process is performed under a condition that an etching selection ratio of said polysilicon layer to said insulating film is in a range of 20 to 40.

4. (Original) A polysilicon etching method according to claim 3, wherein said second plasma etching process is performed at a radio frequency bias power in a range of 10 to 20 W.

5. (Original) A polysilicon etching method according to claim 1, further comprising a step of performing a third plasma etching process after removing the

polysilicon residues, said third plasma etching process being an over-etching process using said resist layer as a mask and mixture gas of HBr or Cl_2, and O_2 as etching gas.

6. (New) A polysilicon etching method comprising steps of:

preparing a semiconductor substrate having an insulating film, and a first polysilicon layer patterned, formed on said substrate and covered with a partial insulating film, and a second polysilicon layer deposited over said first polysilicon layer;

forming a resist layer on said second polysilicon layer, said resist layer having a predetermined pattern not covering at least a portion of side walls of the said first polysilicon layer;

performing a first plasma etching process of etching the said second polysilicon layer by using mixture gas of HBr and Cl_2 and said resist layer as a mask to leave the said second polysilicon layer having a pattern corresponding to said resist layer and polysilicon residues made of a portion of said second polysilicon layer on the said wall;

performing a second plasma etching process by using single gas of HBr and said resist layer as a mask to remove the polysilicon residues so as to make a stacked gate electrode; and

removing said resist layer.

7. (New) A method for manufacturing a semiconductor memory comprising steps of:

preparing a semiconductor substrate having an insulating film, and protrusions by a first polysilicon feature formed on said substrate and covered with a partial insulating film, and a second polysilicon features deposited over said insulating firma and said protrusions;

forming a resist layer on said second polysilicon features, said resist layer having a predetermined pattern not covering at least a portion of side walls of the said protrusions;

performing a first plasma etching process of etching the said second polysilicon features by using mixture gas of HBr and Cl_2 and said resist layer as a mask to leave the said second polysilicon features having a pattern corresponding to said resist layer and polysilicon residues made of a portion of said second polysilicon features on the said wall;

performing a second plasma etching process by using single gas of HBr said resist layer as a mask to remove the polysilicon residues so as to make a stacked gate electrode; and

removing said resist layer.